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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,358	04/19/2004	Show-Nan Chung	CHUN3076/EM	1073

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,358	CHUNG ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, in view of Lovett et al (US Patent 7106637), further in view of Mills et al (6564285).

For claim 1, AAPA teaches the following limitations:

operating both an M-DOC series flash memory and a non-X86 system processor in synchronism (applicant admits that M-DOC series flash memory and non-X86 processors work together)

AAPA does not teach:

Auxiliary device comprising: a first logic circuit enabled by a first address line of the non-X86 system processor for changing output thereof from a first level to a second level; a delay circuit for delaying the second level output of the first logic circuit a predetermined period of time prior to clearing the first logic circuit for changing output thereof from a second level to a first level; and a second logic circuit for performing a logical operation

on the output of the first logic circuit and a CS pin of the non-X86 system processor prior to coupling to a CS pin of the M-DOC series flash memory.

Lovett et al teach the following limitations:

device for operating memory and processor in synchronism comprising:

a first logic circuit enabled by a first address line of the system processor for changing output thereof from a first level to a second level (102a); a delay circuit (106) for delaying the second level output of the first logic circuit a predetermined period of time prior to clearing the first logic circuit for changing output thereof from a second level to a first level (Fig 2 shows ATD_IN is connected to all delay stages. Therefore, delay circuit delays for a period prior to clearing the first logic for changing output from second level to first level); and a second logic circuit (506) for performing a logical operation on the output of the first logic circuit and a CS pin of the processor (506 performs logical operation between 510 and 508. 508 comprises command for memory. Therefore, it comprises CS input from the processor).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of AAPA and Lovett et al. One ordinary skill in the art would be motivated to combine the teachings of AAPA and Lovett to enhance the synchronism between memory and processor.

The combination of AAPA and Lovett et al do not teach second logic circuit prior to coupling to CS pin of flash memory.

Mills et al teach an auxiliary device (830) to operate flash (860) and processor (810) in synchronism where a second logic circuit performs logical operation on the output of first logic and a CS pin of processor prior to coupling to a CS pin of flash memory (830 performs the necessary logic operation on CS pin of processor prior to coupling the CS pin of flash through 850. For that a first logic is necessary for generating flash specific signals and the second logic will convert the CS signal to produce CS signal for flash memory based on flash specific signal).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of AAPA, Lovett et al and Mills et al. One ordinary skill in the art would be motivated to combine the teachings of AAPA, Lovett and Mills et al so that a generic flash interface can be used to work with different processors.

For claims 2-5, the combination does not mention that the delay circuit id a plurality of positive edge triggered D-FFs. One ordinary skill in the art would be motivated to implement delay with positive edge triggered D-FF as D-FFs are used for providing delay.

For claim 6, 506 is a decoder, which can be implemented using OR gate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman
Examiner
Art Unit 2116

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LYNNE H. BROWNE
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